--11. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire including a plurality of gate lines formed on the insulating substrate and a plurality of gate electrodes connected to the gate lines;

a gate insulating layer formed on the gate wire;

a plurality of data lines crossing the gate lines formed on the gate insulating layer and made of an amorphous silicon layer, a doped amorphous silicon layer, and a metal layer;

a plurality of channel portions made of the amorphous silicon layer and formed on the gate insulating layer over the gate electrode;

B1

a plurality of source electrodes connected to the data lines wherein at least a portion of the source electrodes are formed on the channel portions;

a plurality of drain electrodes facing the source electrode on the channel portion;

a passivation layer covering the data lines, the channel portions, and the gate insulating layer, having a plurality of contact holes exposing at least a portion of the drain electrodes; and

a plurality of pixel electrodes formed on the passivation layer and connected to the drain electrode through the contact holes.

12. The thin film transistor array panel of claim 11, wherein the amorphous silicon layer of the data lines has at least a portion of the amorphous silicon layer located within the border line of the metal layer of the data lines.

13. The thin film transistor array panel of claim 12, wherein the width of the metal layer is wider than that of the amorphous silicon layer where the amorphous silicon layer of the data lines is located within the border line of the metal layer of the data lines.

14. The thin film transistor array panel of claim 11, wherein the source electrodes and the drain electrodes are made of the doped amorphous layer and the metal layer.

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15. The thin film transistor array panel of claim 11, wherein the gate wire has a double layered structure made out of a first metal layer, which is made of one of Al and Al-Nd, and a second metal layer which is made of one of Mo, Ta, Cr and their alloys.

16. The thin film transistor array panel of claim 15, wherein the metal layer of the data lines, the source electrodes, and the drain electrodes are made of Cr.

17. The thin film transistor array panel of claim 11, wherein the pixel electrodes are made of indium tin oxide (ITO). --

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 11-17 are pending in the application, with claim 11 being the independent claim. Claim 10 is sought to be cancelled without prejudice